High-precision alignment and bonding system for the fabrication of 3-D nanostructures

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***Abstract*—We successfully developed a high-precision wafer alignment and bonding system for the fabrication of a variety of 3-D nanostructures. To control the wafer positions with high accuracy during the wafer-bonding process, we improved upon a design of the conventional mask-alignment stage. A stress sensor was incorporated to measure the load between the two wafers. In addition, the parallelism of the wafers was monitored by an optical interferometry system. To determine alignment errors in both the x and y directions simultaneously, we devised an alignment method consisting of crossed vernier scales. We demonstrated that the new alignment and bonding system allowed us to realize precise 3-D photonic crystals with the alignment inaccuracy of $<$ 100 nm at most, and we show that the best experimental error achieved to date was $<$ 25 nm. As this system has the benefit of more readily and intuitively determining the absolute positions of the two wafers, it can be applied to the fabrication of a wide variety of nanoscale multilayer devices. [2007-0018]**

***Index Terms*—Microassembly, micromachining, nanostructure, nanotechnology, periodic structure, photonic crystal, wafer bonding, 3-D integration.**

I. Introduction

IMPROVEMENTS to the precision of wafer-bonding and alignment techniques at the submicrometer scale have created the potential for the realization of 3-D nanostructures with unprecedented functions, such as complementary mechanical, electronic, and optical nanodevices. There has been much recent interest in 3-D photonic crystals (PCs) [1], [2] that might allow the complete control of light on an ultrasmall scale, which is a key aspect in improving the performance of optical devices. However, 3-D PCs have complex nanostructures in which the refractive index varies in a periodic fashion, and the realization of 3-D PC optical devices requires the arrangement of components with an accuracy of several tens of nanometers [3]. This issue is being addressed by the development of precise alignment and wafer-bonding techniques. The fabrication of 3-D ICs [4], [5] is also composed of active multilayer devices; thus, they too could be fabricated by employing these techniques. High-precision wafer-bonding and alignment technology has proved effective in allowing accurate interconnections to be made between layers.

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Conventional wafer-bonding systems based on standard mask aligners are used to fabricate microstructures, such as microelectromechanical system (MEMS) devices. The mechanical accuracy is insufficient for the assembly of nanostructures in which the misalignment of bonded wafers must be avoided. The alignment process used in the construction of MEMS devices is generally based on the observation of transmission images of simple geometric patterns, with an accuracy in the order of a few micrometers [6]–[8]. Although the most advanced lithographic technologies have already accomplished accuracies of several nanometers with respect to the optical registration between wafers and photomask patterns, the precision of the direct bonding between nanostructures on adjacent wafers is lower. To date, these devices have been aligned using the laser-beam-assisted method [9]. In the laser-beam-assisted method, the relative position of the bonding nanostructures can be determined by the observation of the intensities of the diffraction patterns, which are formed by the two gratings on the wafers. However, it is difficult to align the absolute position of the nanostructures because the same diffraction patterns appear periodically. In addition, the diffraction patterns become complex when multilayer structures are aligned and stacked as described in [9]. Preliminary simulation of the diffraction patterns needs to be done before stacking the multilayer structures. In this paper, we present a novel alignment and bonding system for the assembly of nanostructures. This alignment method has the benefit of more readily and intuitively determining the absolute positions of the multilayer nanostructures and does not use diffraction patterns. Therefore, it can be applied to the fabrication of a wide variety of nanoscale multilayer devices. We demonstrate the fabrication of high-precision 3-D PCs using this system.

II. Development of a New Wafer Alignment and Bonding System

The following features of an alignment and bonding system are necessary for the fabrication of high-precision 3-D nanostructures: precise stages to control both the lateral position of the wafers and the gap between the wafers; a system to ensure good wafer parallelism; a monitoring method to determine easily the relative positions of the two wafers; and an effective procedure to ensure good alignment during the wafer-contact process.

Fig. 1 shows schematically the new system that we have developed. In order to improve the degree of control in the lateral direction, we use piezoelectric actuators with high

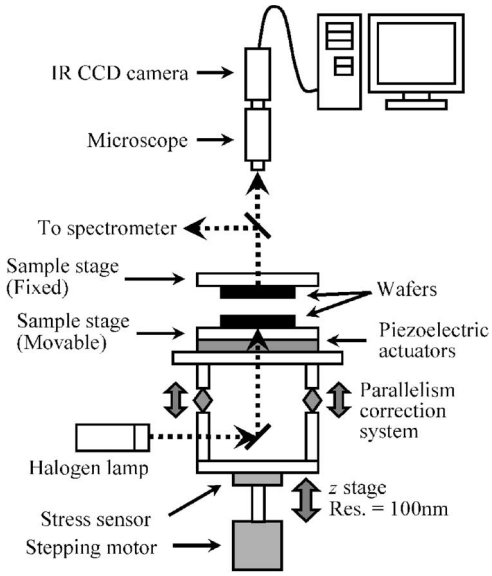

Fig. 1. Schematic illustration of the new high-precision alignment and bonding system.

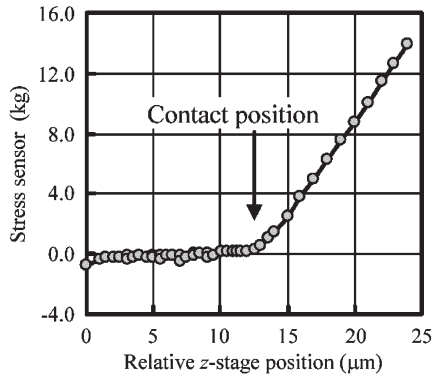

Fig. 2. Measured stress between wafers as a function of relative z-stage position.

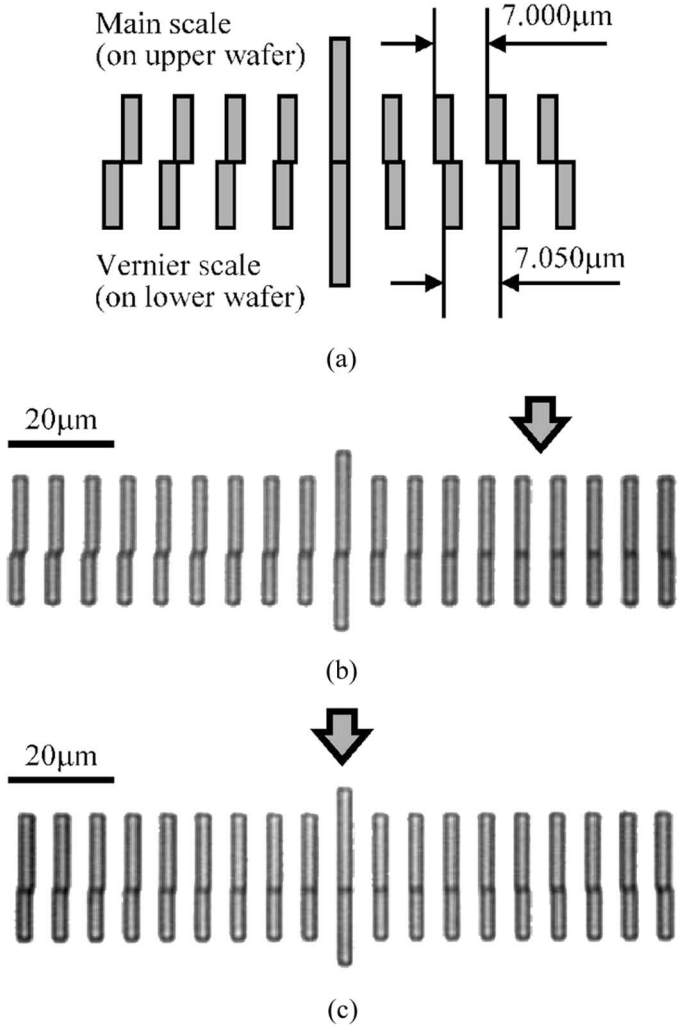

Fig. 3. (a) Schematic illustration of the main and vernier scales. (b) Example of an infrared-transmission image of the scales. The vernier scale is in line with the main scale at the position indicated by the arrow. The lower wafer is located to the left of the upper wafer, and the misalignment is between 250 and 300 nm. (c) Another example of an infrared-transmission image of the scales. The center graduation of the vernier scale is in line with that of the main scale, as indicated by the arrow; therefore, the wafer misalignment is < 50 nm.

resolution and high linearity. The ambient temperature can be controlled to within 0.2 °C to avoid unintentional stretching of the actuators.

The lateral alignment of the wafers should be performed when the gap between them is small, in order to eliminate errors arising from the depth of focus when we observe the alignment patterns on the two wafers. In addition, it was difficult to determine the moment of contact between the wafers clearly. Therefore, the z-stage minimum resolution was improved to 100 nm, and a stress sensor was added to the system to measure the load between the wafers. Fig. 2 shows the relationship between the z-stage position and the measured stress, which is always zero when the wafers are not in contact. After contact has been made, the stress is proportional to the displacement over a relative distance of 12 μm. We can therefore clearly determine the point of initial contact.

We adopted the optical interferometry technique to measure the parallelism between the two wafers. The two wafers are illuminated by a halogen lamp, and the light enters the spectrometer after passing through the gap (Fig. 1). The width of the gap at several different lateral points can be determined from the interference spectra, and we can thus monitor the parallelism. We adjusted the gradient of the sample stage using the measurement results, and the wafers could be made parallel to within 1×10^{-4} rad.

In order to determine the lateral position, we combine a main scale and a vernier scale [Fig. 3(a)]. The periods of the main and vernier scales are 7.000 and 7.050 μm, respectively; thus, the theoretical reading accuracy is 50 nm. The main and vernier patterns are marked on the upper and lower wafers using electron beam lithography and dry etching, respectively. The etched areas are colored gray in Fig. 3(a). The wafers are set on the sample stages, and face-to-face bonding or front-side alignment is performed. The alignment scales are illuminated by the halogen lamp; a transmission image of which is magnified by the microscope and projected onto the charge-coupled device (CCD) camera. We can thus determine the alignment errors

and correct the relative wafer positions using the piezoelectric actuators.

Fig. 3(b) and (c) show examples of transmission images of the scales after the alignment and bonding processes. In these experiments, the wavelength of the transmitted light was in the range of 900–1000 nm and was determined by the transmission bandwidth of the gallium arsenide (GaAs) wafers on which the scales were marked and by the detection bandwidth of the silicon CCD camera. In the case shown in Fig. 3(b), the balance between the vernier scale on the lower wafer and the main scale on the upper wafer is not perfect. The mismatch between the far left graduation marks is greater than that between the far right marks. This indicates that the lower wafer is located slightly to the left of the upper wafer. The graduation marks of both scales are in line at the fifth or sixth mark from the center. This implies that the misalignment of the wafers is 250–300 nm. In the case shown in Fig. 3(c), the balance between the two scales is almost perfect, and the graduation marks are in line close to the center. The wafer misalignment is therefore < 50 nm. These experimental results demonstrate that wafer-alignment accuracy in the order of one-tenth of the observation wavelength can be achieved using the vernier-scale system.

For the practical fabrication of a nanostructure, the main and vernier scales should be placed at four positions in order to determine the alignment errors in both lateral directions. However, even if the alignment process is carried out perfectly, problems can occasionally arise when the z-stage is moved up to bond the wafers. If the parallelism of the wafers is imperfect, the initial contact will take place at an edge, and stress will cause them to slip in the lateral direction. To address this issue, we incorporated a feedback procedure as follows. The z-stage is raised by a single step of the motor; the alignment error is determined from the scales; and the lateral position is adjusted using the piezoelectric actuators. The stage is then raised by another step, and the process is repeated until the wafers are bonded and fixed. In practice, it would be ideal if the alignment errors in both the x and y directions were simultaneously visible. Because the scales are each 150 μm wide, it is more convenient to combine them into a crossed pattern, allowing both to be seen at once, at the same resolution as before.

We thus incorporated new crossed alignment scales using the vernier principle [Fig. 4(a)], which allows the misalignment in both lateral directions to be determined. The difference in pitch between the scales is again 50 nm. The graduations of the main scales are marked on the upper wafer, and the graduations of the vernier scales on the lower wafer are optically placed on each side of the main scale. For the practical fabrication of a nanostructure, the alignment procedure is as follows: First, the wafers are aligned using the four original linear scales; second, the z-stage is raised, and alignment is simultaneously carried out in both the x and y directions using the crossed scales; and third, the precise alignment and bonding process is completed by repeating the second step until the wafers are fixed. Fig. 4(b) shows an experimental example of an infrared-transmission image of the crossed scales after the alignment and bonding process. In this case, the misalignment has been suppressed to < 100 nm.

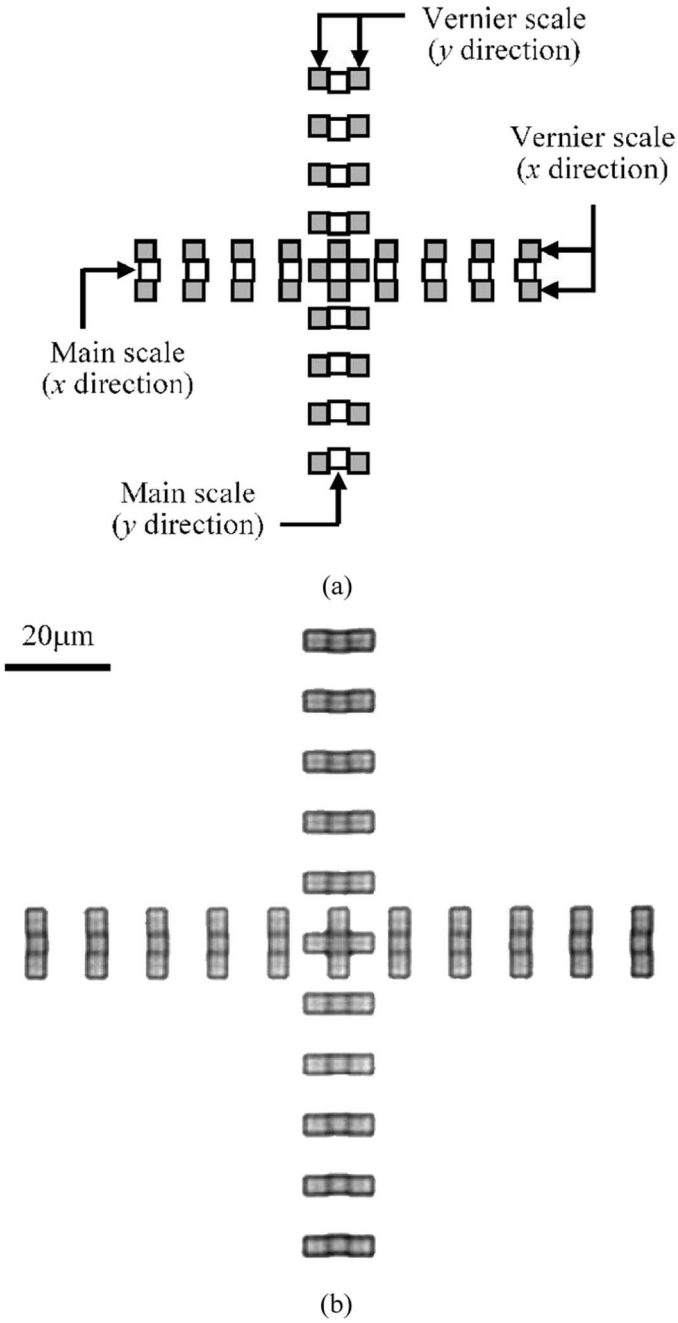

Fig. 4. (a) Schematic layout of the crossed alignment marks. (b) Example of an infrared-transmission image of the crossed scales after the alignment and bonding process.

III. Demonstration of 3-D PC Fabrication Using the New System

We next demonstrated the fabrication of 3-D PCs using the new system described above in combination with the wafer-fusion technique [1], [2], [9], [10]. The PC's stripe structures with a period of 700 nm and a width of 180 nm were formed on GaAs wafers using electron beam lithography and inductively coupled plasma etching with hydrogen iodide and xenon-mixed gases. To stack these stripe structures, high-precision fabrication techniques are needed, as the stripe structure of each layer should be exactly orthogonal to that of the neighboring layers. In addition, the first and third layers should be

precisely aligned such that the lateral distance between the first layer stripes and the third layer stripes is exactly one-half of a stripe period. The second and fourth layers should also be correspondingly aligned. To realize such precise 3-D nanostructures, ideally, the wafers should strongly bond at the moment of contact after being aligned, so-called room temperature bonding. Therefore, the pretreatment process was applied to make the wafers hydrophilic surfaces, allowing them to bond strongly at the moment of contact and avoiding possible displacements due to unavoidable impacts when transferring it to an annealing chamber. The wafers aligned and stacked by the new system were heated to 220 °C under vacuum conditions for up to 24 hours and then fused at 500 °C under H_2 atmosphere for 2–4 h. We also fabricated the degassing channels around the PC regions to funnel away the gas generated from the wafer interface during the annealing process. Scanning acoustic microscopy was employed to investigate the impact of the annealing process [10]. One side of the fused GaAs substrate was mechanically thinned and selectively removed by both wet and dry etching [9]. We thus obtained a two-layer stacked stripe structure. A pair of these were precisely aligned and stacked again, obtaining the four-layer 3-D PC. Fig. 5(a) shows a SEM image of the four-layer 3-D PC after removing one side substrate. In this particular case, the alignment accuracy is < 25 nm. We next prepared a 3-D PC with a so-called acceptor-type defect [11], [12] by removing one stripe period in both directions in each layer. The layers were stacked with high accuracy such that the centers of the defects overlapped with each other. Fig. 5(b) shows a SEM image of the resulting four-layer 3-D PC containing an acceptor-type defect. In this particular sample, the controlled arrangement of the stripes and defects had an error range of < 70 nm, still under the 100-nm maximum. This result indicates that we are not only able to reduce the degradation of the optical properties due to structural fluctuations [3] but can also realize a variety of different 3-D PC devices with advanced functionality by incorporating complex and multilayer defects [12]–[14].

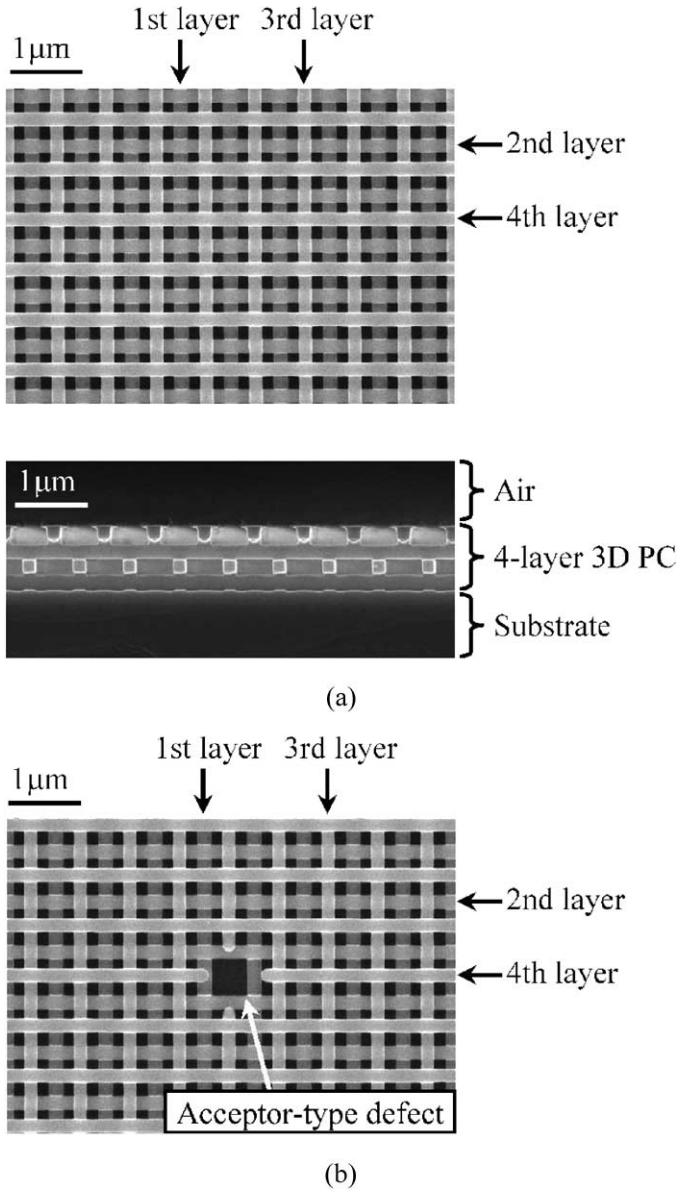

Fig. 5. (a) Top view SEM image of a four-layer 3-D PC (upper) and cross-sectional SEM image of a four-layer 3-D PC (lower). (b) Top view SEM image of a four-layer 3-D PC containing an acceptor-type defect.

IV. Conclusion

We successfully developed a high-precision alignment and bonding system for the fabrication of nanostructures by improving the design of the conventional mask aligner and introducing a new alignment method. The sample stages of the equipment were improved to enable the adjustment of the x, y, and θ positions, and the wafer gap, with high accuracy. A stress sensor was incorporated to measure the load between the two wafers. In addition, the parallelism of the wafers was monitored by an optical interferometry system. We also devised the alignment method which consisted of crossed vernier scales. This allows us to determine alignment errors in both the x and y directions simultaneously. We demonstrated that the new alignment and bonding system allowed us to realize precise 3-D PC with the alignment accuracy of < 100 nm at most. Moreover, if the sample materials could transmit shorter wavelengths such as visible or ultraviolet light, even greater accuracy would be possible because of the improved optical resolution. This precise alignment and bonding system can be used not only for the construction of 3-D PCs and the stacking of 3-D ICs but also for the fabrication of a range of nanostructures, such as complementary mechanical, electronic, and optical nanodevices.

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